WHAT IS CLAIMED IS:

1. A data processing system comprising:

an erasable and programmable non-volatile memory; and

a central processing unit;

wherein the central processing unit executes a predetermined process to thereby carry out a process for increasing the number of assurances for rewriting in a specified partial storage area of the non-volatile memory as compared with the number of assurances for rewriting in other storage areas of the non-volatile memory.

2. A data processing system comprising:

an erasable and programmable non-volatile memory; and

a central processing unit;

wherein the central processing unit executes a predetermined process to thereby generate error correcting information and add the same to data to be written in a specified partial storage area of the non-volatile memory and allow an error decision and an error correction based on the error correcting information to be effected on the data read from the specified partial storage area.

3. The data processing system according to claim 2,

which is a single chip type microcomputer wherein the non-volatile memory and the central processing unit are formed on a single semiconductor chip.

4. The data processing system according to claim 2, which is configured in a multi-chip form wherein the non-volatile memory and the central processing unit are respectively formed on discrete semiconductor chips.

5. The data processing system according to claim 2, wherein the predetermined process comprises an error-correcting information generating program for generating error correcting information for the data written into the specified partial storage area of the non-volatile memory, and an error-correcting program for effecting an error decision and an error correction on data with error correcting information read from the specified partial storage area.

6. The data processing system according to claim 5, which has a storage area for a matrix table wherein when the data is configured as n bits and error correcting information for the n-bit data is defined as m bits, mutually-different binary numbers of m bits are arranged in an m+n array, and wherein the matrix table is referred to the error-correcting information generating program and the error-correcting program.

7. The data processing system according to claim 5, further including a mask ROM accessible by the central processing unit, and wherein the mask ROM has the error-correcting information generating program and the error-correcting program.

8. The data processing system according to claim 5, wherein the other storage areas of the non-volatile memory have areas for storing the error-correcting information generating program and the error-correcting program.

9. The data processing system according to claim 8, wherein the other storage areas of the non-volatile memory have an erase prohibition area in which an erase operation is prohibited, and a rewrite allowable area in which erasing and writing are allowed, and the areas for storing the error-correcting information generating program and the error-correcting program are assigned to the erase prohibition area.

10. The data processing system according to claim 9, wherein the error-correcting information generating program serves so as to generate error correcting information and thereafter store the generated error correcting information and data corresponding thereto in

the specified partial storage area in accordance with a prescribed format as data with the error correcting information, and the error-correcting program serves so as to recognize the data with the error correcting information in accordance with the prescribed format.

11. The data processing system according to claim 8, wherein the other storage areas of the non-volatile memory have an erase prohibition area in which an erase operation is prohibited, and a rewrite allowable area in which erasing and writing are allowed, and the areas for storing the error-correcting information generating program and the error-correcting program are assigned to the rewrite allowable area.

12. The data processing system according to claim 5, further including a RAM to which the error-correcting information generating program and the error-correcting program are transferred from the non-volatile memory, and wherein the central processing unit executes the error-correcting information generating program and the error-correcting program transferred to the RAM.

13. The data processing system according to claim 12, wherein the central processing unit transfers the error-correcting information generating program and the error-correcting program from the non-volatile memory to

the RAM in response to reset instructions.

14. The data processing system according to claim 5, further including a RAM accessible by the central processing unit, and wherein the central processing unit successively reads data with error correcting information from the partial storage area of the non-volatile memory in response to reset instructions, effects the error decision and error correction on the read data with error correcting information according to the execution of the error-correcting program, and initially stores the data subjected to the error decision and correction in the RAM.

15. The data processing system according to claim 5, wherein the central processing unit has means for holding information indicative of the occurrence of an error uncorrectable in the error determining process under the execution of the error-correcting program, recognizably from the outside.

16. A data processing system comprising:

a first storage area low in the number of rewrite assurances; and

a second storage area high in the number of rewrite assurances, both being provided in an address space of an arithmetic control device,

wherein the first storage area comprises an ECC

code generating program for generating each of ECC codes for data to be written in the second storage area, and an error-correcting program for effecting an error decision and an error correction on data with the ECC codes read from the second storage area, and the arithmetic control device executes the ECC code generating program when data is stored in the second storage area.

17. The data processing system according to claim 16, wherein the arithmetic control device executes the error-correcting program when the corresponding data is read from the second storage area.

18. The data processing system according to claim 16, wherein the arithmetic control device is capable of executing the error-correcting program in response to a predetermined operation mode and sequentially transferring the data of the second storage area to the RAM in advance.

19. The data processing system according to claim 16, wherein the first storage area is a mask ROM, and the second storage area is an electrically erasable and programmable flash memory.

20. The data processing system according to claim 16, wherein each of the first storage area and the second

storage area is an electrically erasable and programmable flash memory, the flash memory has a write/erase program for the flash memory, and further including a RAM to which the write/erase program is transferred from the flash memory, and wherein the arithmetic control device is capable of executing the write/erase program placed on the RAM in response to a specific operation mode.

21. A data processing method using a matrix table wherein when ECC codes are defined as m bits with respect to data of n bits, mutually-different binary numbers of m bits are arranged in an m+n array, comprising:

exclusive-ORing values in columns of the matrix table, corresponding to bit positions of logical values "1" of data every bits as viewed in a row direction upon generating the ECC codes;

setting the values of m bits obtained from the exclusive-ORing as the ECC codes; and

adding the ECC codes to data respectively to thereby generate code words of m+n bits.

22. The data processing method according to claim 21, further comprising exclusive-ORing values in columns of the matrix table, corresponding to bit positions of logical values "1" of the code words every bits as viewed in the row direction, making an error-free decision when the values of m bits obtained by the exclusive-ORing are

of a logical value "0" in all bits to thereby set the n-bit data of the cord words as normal data, determining that an error exists when the values of m bits obtained by the exclusive-ORing are of a logical value "1" even one bit, retrieving a column coincident with a binary number of m bits obtained by the exclusive-ORing from the columns of the matrix table, inverting bits of code words at positions associated with the retrieved column in logical value and correcting the same, and defining the n-bit data of the corrected code words as normal data.

23. The data processing system according to claim 7, wherein the central processing unit has a storage circuit for holding, when error-correctable data is detected during the execution of the error-correcting program, information corresponding to the result of detection.

24. The data processing system according to claim 23, wherein the information corresponding to the result of detection is used as warning information.

25. A semiconductor integrated circuit comprising:

a CPU; and

an erasable and programmable non-volatile memory;

wherein the CPU is capable of storing one data in memory cells at different addresses when information is written in a specific block corresponding to part of a

storage area in the non-volatile memory, reading data from the memory cells at the different addresses when data is read from the specific block, and performing a logical operation on the read plural data to thereby effect a necessary error correction to the data.

26. The semiconductor integrated circuit according to claim 25, wherein the number of the different addresses is two or more, and the logical operation is a logical OR operation based on the execution of an instruction included in an instruction set of the CPU.

27. The semiconductor integrated circuit according to claim 25, wherein the number of the different addresses is two or more, and the logical operation is a logical AND operation based on the execution of an instruction included in an instruction set of the CPU.

28. The semiconductor integrated circuit according to claim 25, wherein the number of the different addresses is three or more, and the logical operation is an operation for effecting majority decision on the plural data read from the memory cells at the different addresses.

29. The semiconductor integrated circuit according to claim 25, wherein the non-volatile memory has a

program area for storing a program executed by the CPU, as an area different from the specific block.

30. The semiconductor integrated circuit according to claim 29, wherein the program area includes a program for storing the one data in the memory cells at the different addresses, a program for performing the error correction, and other programs.

31. The semiconductor integrated circuit according to claim 25, wherein the specific block has a product spec for assuring the number of rewritings greater than other blocks.

32. The semiconductor integrated circuit according to claim 25, wherein the non-volatile memory is a flash memory capable of storing information therein according to high and low levels of a threshold voltage of each memory cell.

33. The semiconductor integrated circuit according to claim 25, wherein the CPU and the non-volatile memory are formed on a single semiconductor chip which constitutes a microcomputer.

34. The semiconductor integrated circuit according to claim 25, wherein the CPU and the non-volatile memory

are respectively formed on separate semiconductor chips.